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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,345	12/29/2003	Mark L. Doczy	42P17820	8139

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

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06/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/748,345	DOCZY ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,11-13,15,16 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,11-13,15,16 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/29/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed 4/30/07.

Claims **1-2, 4-8, 11-13, 15-16** and **25** are pending in this application.

Claims **3, 9-10, 14 and 17-24** have been cancelled.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 5, 7-8, 11-13, 15-16 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by En et al. (6,713,819).

Regarding claims 1, 5, 7-8, 12, 16 and 25, En et al. disclose (see specifically figures 1-3) a method of forming a microelectronic structure comprising: providing a substrate (10) comprising source/drain regions (22/24, 40/42) and gate region (32/54), wherein the gate region comprises a metal layer (36/54) of tungsten, ruthenium, palladium, or platinum (Col. 3, lines 58+ and Col. 4, lines 39+) disposed directly on a high k gate dielectric layer (38/56/86) of hafnium oxide, zirconium oxide, titanium oxide, or aluminum oxide (Col. 4, lines 10+), wherein a spacer (62/64) is in direct contact with the metal gate layer; laser annealing the substrate to activate the implanted species (Col.

8, lines 33+). En et al. further disclose NMOS gate electrode and a PMOS gate electrode (Col. 3, lines 20+). In addition, En et al.'s figures 3A-3D show the ratio of the depth of the source/drain regions to the length of the source/drain regions being less than about 1:2.

Regarding claims 2, 11, 13, and 15, since En et al. disclose the metal layer (36/54) is made of tungsten, ruthenium, palladium, or platinum as applicant claimed, the work function of at least one of such materials is considered to be in the claimed work function ranges (e.g., from about 3.9 electron volts to about 5.2 electron volts, from about 3.9 electron volts to about 4.2 electron volts, and from about 4.8 electron volts to about 5.1 electron volts).

3. Claims 1-2, 5, 7-8, 11-13, 15-16 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Chambers (7,005,365).

Regarding claims 1-2, 5, 7-8, 11-13, 15-16 and 25, Chambers disclose (see specifically figures 1-3) a method of forming a microelectronic structure comprising: providing a substrate (110/210) comprising source/drain regions (155/160, 255/260) and gate region there between, wherein the gate region comprises a metal layer (125/135, 225/235) of ruthenium, palladium, or platinum (Col. 6, lines 28+ and Col 8, lines 22+) disposed directly on a high k gate dielectric layer (105/205) of hafnium dioxide (Col. 4, lines 58+), wherein a spacer (165/265) is in direct contact with the metal gate layer; laser annealing the substrate to activate the implanted species. Chambers further discloses NMOS gate electrode and a PMOS gate electrode (Col. 1, lines 22+ and Col 6, lines 10+), and the metal gate layer can be selected to have the work function in the range from

about 4 electron volts to about 4.2 electron volts and from about 5 electron volts to about 5.2 electron volts (Col. 6, lines 13+).

4. Claims 1-2, 5, 7-8, 11-13, 15-16 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al. (6,930,335).

Regarding claims 1, 5, 7-8, 12, 16 and 25, Yamaguchi et al. disclose (see specifically figure 1-2) a method of forming a microelectronic structure comprising: providing a substrate (101) comprising source/drain regions (105) and gate region there between, wherein the gate region comprises a metal layer (104) of tungsten, ruthenium, or titanium (Col. 3, lines 38+) disposed directly on a high k gate dielectric layer (103) of hafnium oxide (Col. 4, lines 21+), wherein a spacer (107) is in direct contact with the metal gate layer; laser annealing the substrate to activate the implanted species (Col. 8, lines 5+). Yamaguchi et al.'s figure 1 shows the ratio of the depth of the source/drain regions to the length of the source/drain regions being less than about 1:2.

Regarding claims 2, 11, 13, and 15, since Yamaguchi et al. disclose the metal layer (104) is made of tungsten, ruthenium, or titanium as applicant claimed, the work function of at least one of such materials is considered to be in the claimed work function ranges (e.g., from about 3.9 electron volts to about 5.2 electron volts, from about 3.9 electron volts to about 4.2 electron volts, and from about 4.8 electron volts to about 5.1 electron volts).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over En et al. (6,713,819) in view of Goto (6,599,819 of record).

Regarding claim 6, En et al. disclose the claimed invention as detailed above except for specifying the laser beam pulsed at *about 20 nanoseconds or less.*

Although En et al. do not specify the claimed time range of the laser beam pulsed (e.g., 20 nanoseconds or less), the annealing time using laser beam is commonly less than 20 ns for activating the implanted regions in a substrate, as disclosed by Goto (Col. 3, lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser beam to the substrate at about 20 ns or less for activating the implanted regions in the substrate since such the pulsed time of a laser beam is commonly applied in the art, as taught by Goto, and such time range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over En et al. (6,713,819) in view of Tsukamoto (6,040,224 of record).

Regarding claim 4, En et al. disclose the claimed invention as detailed above except for a polysilicon layer disposed on the metal gate.

Tsukamoto while related to a similar method of forming a microelectronic structure teaches (see specifically figures 5C-5E) a polysilicon layer (16) disposed on the metal gate layer (15), and laser annealing the substrate to activate the implanted species (Col. 4, lines 65+),

wherein the doped polysilicon film (16) is adapted to protect the metal gate layer (15) from the laser annealing (Col. 4, lines 25+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Tsukamoto's teaching with En et al.'s method would have been beneficial because it helps to protect the metal gate layer. As the result, the metal gate is obviously considered "*not substantially diffuse into the gate dielectric layer*".

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chambers (7,005,365) in view of Goto (6,599,819 of record).

Regarding claim 6, Chambers discloses the claimed invention as detailed above except for specifying the laser beam pulsed at *about 20 nanoseconds or less*.

Although Chambers does not specify the claimed time range of the laser beam pulsed (e.g., 20 nanoseconds or less), the annealing time using laser beam is commonly less than 20 ns for activating the implanted regions in a substrate, as disclosed by Goto (Col. 3, lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser beam to the substrate at about 20 ns or less for activating the implanted regions in the substrate since such the pulsed time of a laser beam is commonly applied in the art, as taught by Goto, and such time range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chambers (7,005,365) in view of Tsukamoto (6,040,224 of record).

Regarding claim 4, Chambers discloses the claimed invention as detailed above except for a polysilicon layer disposed on the metal gate.

Tsukamoto while related to a similar method of forming a microelectronic structure teaches (see specifically figures 5C-5E) a polysilicon layer (16) disposed on the metal gate layer (15), and laser annealing the substrate to activate the implanted species (Col. 4, lines 65+), wherein the doped polysilicon film (16) is adapted to protect the metal gate layer (15) from the laser annealing (Col. 4, lines 25+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Tsukamoto's teaching with Chambers's method would have been beneficial because it helps to protect the metal gate layer. As the result, the metal gate is obviously considered "*not substantially diffuse into the gate dielectric layer*".

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (6,930,335) in view of Goto (6,599,819 of record).

Regarding claim 6, Yamaguchi et al. disclose the claimed invention as detailed above except for specifying the laser beam pulsed at *about 20 nanoseconds or less.*

Although Yamaguchi et al. do not specify the claimed time range of the laser beam pulsed (e.g., 20 nanoseconds or less), the annealing time using laser beam is commonly less than 20 ns for activating the implanted regions in a substrate, as disclosed by Goto (Col. 3, lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser beam to the substrate at about 20 ns or less for activating the implanted regions in the substrate since such the pulsed time of a laser beam is commonly applied in the art, as taught by Goto, and such time range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

Conclusion

11. Applicant's arguments with respect to claims **1-2, 4-8, 11-13, 15-16** and **25** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

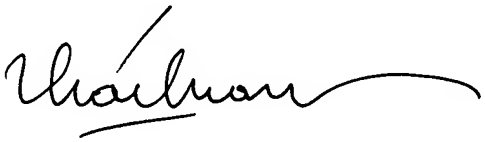
12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the newly added limitations (e.g., the underlined portions) into independent claims 1 and 11 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 8:00 AM - 4:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai
Primary Examiner
Art Unit 2891
June 15, 2007